ABSTRACT OF THE DISCLOSURE

In a layout design method for a semiconductor integrated circuit, a cell layout library is provided which stores structure information of functional cells and a plurality of groups of filler cells, each filler cell acting to fill space between the functional cells. The functional cells are arranged on a layout based on the structural information from the layout library. The filler cells of any of the plurality of groups are arranged selectively based on the structural information from the layout library so that the filler cells are arranged in channel regions where the functional cells are not located on the layout, each channel region being located at a predetermined distance from signal lines on the layout.